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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,911	07/10/2003	Mitsuhiro Higashiho	024016-00065	9535

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EXAMINER	
PHUNG, ANH K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Sepplemental Notice of Allowability	Application No. 10/615,911	Applicant(s) HIGASHIHO, MITSUHIRO	
	Examiner ANH PHUNG	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *9 and 10*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/132,405* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Anh Phung

ANH PHUNG
PRIMARY EXAMINER

Supplemental Office Action

Examiner's amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CAR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The Specification has been amended as follow:

Delete paragraph from line 20 on page 24 to line 5 on page 25;

delete paragraph from line 4 on page 39 to line 14 on page 39;

delete paragraph from line 21 on page 41 to line 6 on page 42; and

delete paragraph from line 24 on page 48 to line 3 on page 49; see attachment sheets.

The examiner's amendment has been made in order to place the application in a condition for allowance as it is improper to make specific reference to claims by number in the "DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS".

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **ANH PHUNG** whose telephone number is **(571) 272-1883**. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD ELMS**, can be reached on **(571) 272-1869**. The fax phone number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

Art Unit: 2824

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Anh Phung

ANH PHUNG
PRIMARY EXAMINER

Attachment Sheets

case where the comparison result indicates the inconsistence (S6: NO). Accordingly, the change-over control can be carried out by the required minimum instructions.

Besides, in the case where the same operation mode is set in a plurality of continuous operation cycles, the change-over control is carried out only in the first operation cycle in the plurality of operation cycles (S6: NO), and the switching control is not carried out in the subsequent operation cycle (S6: YES). After the change-over control is completed in the first operation cycle, the instructions of the unnecessary switching control can be suppressed.

The change-over control of the change-over switch is, for example, change-over of a supply source of the internal signal, and the change-over of the supply source of the internal signal can be carried out without carrying out the unnecessary switching control and by the required minimum control.

~~Here, the mode discriminating section 3 is an example~~ of a mode discriminating section in claim 1, and an example of a mode discriminating circuit in claim 9. Besides, the switch section 6 is an example of a switching section in claim 1, and an example of an address switching circuit in claim 9. Besides, the switch change-over signal SW is an example of a switching control signal in claims 1 and 9. Besides, the mode record holding section 4 and the comparator section 5 constitute a switching control section in claim 1, and constitute a switching control circuit in claim 9. Among these, the mode record holding section 4 is

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delete 2/10/06 ~~an example of a recording section in claim 2.~~

~~Besides, S3 and S4 in the flowchart of Fig. 3 express an example of a mode discriminating process in claim 11, and S5 to S8 express an example of a switching control process in claim 11.~~

Next, a description will be given of a case where a semiconductor memory device 10 of a second embodiment is applied to a pseudo-SRAM as a DRAM having a built-in refresh operation. This is an application example to an address switching control between two modes of an ordinary data-input/output mode and a refresh mode. In Fig. 4, there is provided an address switching circuit 13 to which a refresh address ADD (Ref) from a refresh address counter 14 for supplying an address at the time of a refresh mode and an external address ADD (R/W) inputted from the outside at the time of an ordinary data-input/output mode are inputted, and which propagates one of them to an internal address ADD (Int). The internal address ADD (Int) to which one of the refresh address ADD (Ref) and the external address ADD (R/W) is propagated, is inputted to a decoding circuit 15, and controls, as a decoding signal AD, a memory cell array 16.

Besides, there are provided a mode discriminating circuit 11 to which instruction signals of two operation modes, i.e., a refresh operation requesting signal REQ (Ref) and a data-input/output requesting signal REQ (R/W) are inputted, and a switch holding circuit 12 to which a mode discriminating signal M outputted from the mode discriminating circuit 11 and the data-input/output requesting signal REQ (R/W) are inputted. A switch

cycle, and the unnecessary switching resulting from that are prevented from occurring, and the electric current consumption can be suppressed to be minimum.

~~Here, the mode discriminating circuit 11 is an example~~ of the mode discriminating section in claim 1, and an example of the mode discriminating circuit in claim 9. Besides, the address switching circuit 13 is an example of the switching section in claim 1, and is an example of the address switching circuit in claim 9. Besides, the switch change-over signal (S) is an example of the switching control signal in claims 1 and 9. Besides, the switch holding circuit 12 is the switching control section in claim 1, and is the switching control circuit in claim 9. Besides, it ~~is an example of the recording section in claim 2.~~

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In a system configuration diagram 2 for realizing a control method of a third embodiment shown in Fig. 9, in addition to the system configuration diagram 1 of the first embodiment, there are provided a decoder 1(7) for decoding an upper signal, and a decoder 2(8) for further decoding the output signal of the decoder 1(7) added with a lower signal. The output signals of the decoder 1(7) and the decoder 2(8) are inputted to a switch section 6.

Incidentally, in the description here, structural elements having the same function and the same operation and effect as the structural elements in the system configuration diagram 1 of the first embodiment are designated by the same symbols, and the description here is omitted.

In the system configuration diagram 2, a decode width of an input signal propagated to an internal signal varies

concerning the control method of the first embodiment are designated by the same step numbers, and the description here is omitted. In Fig. 10, instead of S2 and S7 in the flowchart (Fig. 3) of the first embodiment, steps of S22 and S27 are included. At the step S22, the bit number of a signal to be decoded is initialized in accordance with the initialization of an operation mode record. Besides, at the step S27, when the operation mode corresponding to the input is not coincident with the operation mode record, the bit number of a signal to be decoded is changed.

The control method of the third embodiment as described above has the same operation and effect as the control method of the first embodiment. Here, the control of the bit number of the signal to be decoded is such that for example, in a signal composed of a plurality of bits, a decoded bit number is switched, and the decode result is propagated to the internal signal. The unnecessary switching control is not carried out, and switching of the decoding signal to the internal signal can be carried out by the required minimum control.

~~Here, the mode discriminating section 3 is an example~~ of the mode discriminating section in claim 1, and is an example of the mode discriminating circuit in claim 10. Besides, the switch section 6 is an example of the switching section in claim 1. The switch change-over signal SW is an example of the switching control signal in claims 1 and 10. Besides, the mode record holding section 4 and the comparator section 5 constitute the switching control section in claim 1, and constitute the switching control circuit in claim 10. Among them, the mode record holding

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~~section 4 is an example of the recording section in claim 2.~~

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~~Besides, S3 and S4 in the flowchart of Fig. 10 are an example of the mode discriminating process in claim 12, and S5, S6, S27 and S8 are an example of the switching control process in claim 12.~~

Here, before a description of a case where a semiconductor memory device 20 of a fourth embodiment in Fig. 12 is applied to a pseudo-SRAM as a DRAM having a built-in refresh operation, a memory cell array MARY structure of the pseudo-SRAM will be described with reference to Fig. 11. The memory cell array MARY in which memory cells are arranged in a matrix form is divided in a row direction and a column direction with a predetermined length and is constituted by, as one unit, a memory cell block MBx. In the row direction, the control is carried out by a row decoder RDEC to which the decoding signal AD decoded by the decoding circuit 15 is inputted, and in the column direction, the control is carried out by a column decoder CDEC. By these controls, the memory cell block MBx is selected. Specifically, a main word line MWL is selected by a main word driver MWD in the row decoder RDEC. Besides, by a block selecting signal CBx (x = 0 to 7) outputted from the column decoder CDEC, a position of the memory cell block MBx activated in the column direction is selected. By a sub-word driver SWD arranged at the column position selected by this block selecting signal CBx (X = 0 to 7), a sub-word line SWL is activated on the basis of the activation signal from the main word line MWL. Memory cell information is read out to a bit line BL or /BL, and is

From the above, an unnecessary switch change-over signal SW is not outputted, and the block decoding circuit 23 can be controlled by the output of the required minimum switch change-over signal SW. Besides, the bit number of the address connected to the block decoding circuit 23 is switched, the block selecting signal CBx is changed, and the memory cell array block MBx to be accessed is set, so that the memory cell array block MBx is not unnecessarily switched. Thus, unnecessary circuit operations in respective circuits leading to the memory cell can be prevented. Besides, unnecessary driving of the block selecting signal CBx from the block decoding circuit 23 can be reduced. Accordingly, the output of the unnecessary switch change-over signal SW at every operation cycle, and the unnecessary switching of the block selecting signal CBx resulting from that are prevented from occurring, and the current consumption can be suppressed to be minimum.

Besides, the predetermined low order bit position is a lower order bit position in the data input/output mode as compared with a bit position in the refresh mode, so that an address region set in the refresh mode can be made wider, and an address region set in the data-input/output mode can be made narrower.

~~Here, the mode discriminating circuit 11 is an example~~ of the mode discriminating section in claim 1, and is an example of the mode discriminating circuit in claim 10. Besides, the block decoding circuit 23 is an example of the switching section in claim 1. The switch change-over signal SW is an example of the switching control signal in claims 1 and 10. Besides, the switch holding circuit 12 constitutes

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~~the switching control section in claim 1, and constitutes the switching control circuit in claim 10. It is an example of the recording section in claim 2.~~

By applying the semiconductor memory devices 10 and 20 of the second and fourth embodiments as described above in combination, in the DRAM such as the pseudo-SRAM, the ratio of the consumed electric current at the time of the refresh operation to the stand-by current can be reduced to approximately a half or less as compared with the case of the background art.

Further, in the first and second embodiments, at the time of the start of the operation cycle or a subsequent suitable timing, the operation mode is compared with the operation mode of the former operation cycle, and a suitable switching-procedure instruction is given in accordance with the result. There is no unnecessary switching-procedure instruction, and the switching control can be carried out by the required minimum switching-procedure instruction.

Besides, since the switching-procedure instruction is given only in the case where the comparison results are inconsistent, the unnecessary switching-procedure instruction can be suppressed.

Besides, in the case where the same operation mode is set in a plurality of continuous operation cycles, since the switching-procedure instruction is given only at the first operation cycle in the plurality of operation cycles, after the switching procedure is completed at the first operation cycle, the unnecessary switching-procedure instruction can be suppressed.